

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant: Matthias Muth

Group Art Unit: 2183

Serial No.: 10/517,284

Examiner: Faherty, Corey S.

Filed: December 8, 2004

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For: METHOD AND BASE CHIP FOR MONITORING THE OPERATION OF A
MICROCONTROLLER UNIT

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37(a)

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner dated January 13, 2010, which finally rejected claims 1 and 3-13 in the above-identified application. A Notice of Appeal was filed on May 13, 2010 along with a Pre-Appeal Brief Request for Review. A panel decision on the Pre-Appeal Brief Request for Review was notified on July 9, 2010. This Appeal Brief is hereby submitted pursuant to 37 C.F.R. § 41.37(a).

Petition is hereby made under 37 C.F.R. 1.136(a) to extend the time for filing this Appeal Brief to and through September 9, 2010, comprising an extension of time by one month (\$130) from August 9, 2010, which is the end of the one month time period from mailing of the decision of the pre-appeal brief request.

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I. REAL PARTY IN INTEREST

The real party in interest in this appeal is NXP B.V., High Tech Campus 60, 5656 AG Eindhoven, The Netherlands.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.

III. STATUS OF CLAIMS

Claims 1-10 were originally filed on December 8, 2004. In a preliminary amendment filed on December 8, 2004, claims 1-10 were amended and new claims 11-13 were added. In response to the Non-Final Office Action of June 10, 2008, claims 1, 3, 5-7, 10 and 11 were amended and claim 2 was canceled. In response to the Final Office Action of October 7, 2008, claims 1 and 5 were amended. In response to the Non-Final Office Action of January 13, 2009, claims 1 and 5 were amended. In response to the Final Office Action of March 31, 2009, claims 1 and 3-6 were amended. Claims 1 and 3-13 stand finally rejected and form the subject matter of the present appeal.

Claims 1-8 and 17-28 stand rejected as follows:

Claims 1, 3, 5 and 9-13 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Stolan (U.S. Pat. No. 5,864,663) in view of Juzswik (U.S. Pat. No. 4,698,478).

Claims 4 and 6-8 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Stolan in view of Juzswik and further in view of Ubicom (Ubicom Product Report –IP2022 Internet Processor, hereinafter “Ubicom”).

A copy of the claims is set forth in the Claims Appendix.

IV. STATUS OF AMENDMENTS

No amendments were filed subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This section of this Appeal Brief is set forth to comply with the requirements of 37 C.F.R. § 41.37(c)(1)(v) and is not intended to limit the scope of the claims in any way. Examples of implementations of the limitations of independent claims 1 and 5 are described below.

The language of claim 1 relates to a method of monitoring the operation of a microcontroller unit (300) that is intended for at least one application and is associated with a system (100), by means of a base chip (200), particularly a system base chip (Page 1, lines 1-3 and page 5, line 31 - page 6, line 2; Figs. 1 and 2). The method is characterized in that: causing a reset (R) of the microcontroller unit (300) if a reset condition is detected, wherein the reset condition is transmission of at least one special sequence, particularly at least one drive or access sequence assigned to the reset operation, to the base chip and the reset (R) of the microcontroller unit (300) is confirmed under an enquiry routine by checking whether the at least one special sequence has been successfully transmitted to the base chip (200) (Page 3, lines 7-10 and 15-21 and page 5, line 31 - page 6, line 8; Figs. 1 and 2); activating a special mode of operation (S), particularly a flash mode of the base chip (200), once after the check has been made to see whether the special sequence has been successfully applied and after the reset operation, by allowing access to a monitoring module (10) that is associated with the base chip to take place in a manner which is simplified in comparison with the normal mode of operation (N) of the microcontroller unit (300) (Page 3, lines 28-32 and page 6, lines 9-32; Figs. 1 and 2); supplying a permanent energy supply from a battery unit (400) to the monitoring module (10) (Page 5, lines 20-27; Fig. 1); and switching a microcontroller supply unit (50) of the base chip (200) to enable or disable a temporary energy supply from the battery unit (400) to the microcontroller unit (300) (Page 5, lines 20-27; Fig. 1).

The language of claim 5 relates to a base chip (200), particularly a system base chip, for monitoring the operation of a microcontroller unit (300) that is intended for at least one application (Page 1, lines 4-6 and page 5, lines 8-11; Figs. 1 and 2). The base chip (200) is characterized in that: a reset unit (40) for resetting (R) the microcontroller unit (300), which reset unit is connected to said microcontroller unit (300), wherein a reset (R) of the microcontroller unit (300) is caused if a reset condition is detected,

wherein the reset condition is transmission of at least one special sequence, particularly at least one drive or access sequence assigned to the reset operation, to the base chip (200) and the reset (R) of the microcontroller unit (300) is confirmed under an enquiry routine by checking whether the at least one special sequence has been successfully transmitted to the base chip (200) (Page 3, lines 7-10 and 15-21, page 5, lines 12-16, and page 5, line 31 - page 6, line 8; Figs. 1 and 2); a microcontroller supply unit (50) connected to the microcontroller unit (300), wherein the microcontroller supply unit (50) is permanently associated with a battery unit (400) (Page 5, lines 20-27; Fig. 1); a switch (54) connected to the microcontroller supply unit (50), wherein the switch (54) is configured to switch the microcontroller supply unit (50) to enable or disable a temporary energy supply from the battery unit (400) to the microcontroller unit (300) (Page 5, lines 20-27; Fig. 1); a monitoring module (10) that is associated with the microcontroller unit (300), wherein a special mode of operation (S), particularly a flash mode of the base chip (200), can be activated once after the check has been made to see whether the special sequence has been successfully applied and after the reset operation (R), by allowing access to the monitoring module (10) to take place in a manner which is simplified in comparison with the normal mode of operation (N) of the microcontroller unit (300), wherein the monitoring module (10) is permanently associated with the battery unit (400) so that the monitoring module (10) receives a permanent energy supply from the battery unit (400) (Page 3, lines 28-32, page 5, lines 20-27 and page 6, lines 9-32; Figs. 1 and 2).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

- A. Whether or not independent claim 1 is unpatentable over Stolan in view of Juzswik under 35 U.S.C. 103(a).
- B. Whether or not independent claim 5 is unpatentable over Stolan in view of Juzswik under 35 U.S.C. 103(a).
- C. Whether or not dependent claims 3, 4 and 6-13 are unpatentable over Stolan in view of Juzswik under 35 U.S.C. 103(a) or unpatentable over Stolan in view of Juzswik and further in view of Ubicom under 35 U.S.C. 103(a).

VII. ARGUMENT

A. Independent claim 1 is patentable over Stolan in view of Juzswik under 35 U.S.C. 103(a).

Appellant respectfully submits that a *prima facie* case of obviousness has not been established with respect to claim 1. Appellant respectfully asserts that the Examiner has failed to provide *prima facie* support for the obviousness rejection. In addition, Appellant respectfully asserts that one skilled in the art would not combine the teachings of Stolan and Juzswik to derive the claimed invention as suggested by the Examiner.

Examiner has failed to provide *prima facie* support for the obviousness rejection.

In the Final Office Action on page 3, the Examiner correctly recognizes that “Stolan does not explicitly disclose the steps of supplying a permanent energy supply from a battery unit to the monitoring module; and switching a microcontroller supply unit of the base chip to enable or disable a temporary energy supply from the battery unit to the microcontroller unit.” The Examiner then alleges that “Juzswik discloses using this technique [col. 2, line 32 – col. 3, line 4] for the purpose of reducing power consumption in a system having a microprocessor and a watchdog timer” and concludes that “[s]uch operation would therefore have been obvious in the system of Stolan.” However, Appellant respectfully asserts that the Examiner has failed to provide *prima facie* support for the obviousness rejection.

As the MPEP makes clear, “[t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The supreme Court in *KSR International Co. v. Teleflex Inc.*, 550 U.S. __, __, 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Federal Circuit has stated that ‘rejections based on obviousness cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.’ *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006).” MPEP §2142.

However, the only statement made by the Examiner in support of an obviousness rejection of claim 1 is that “[s]uch operation would therefore have been obvious in the

system of Stolan,” which is a mere conclusory statement and fails to clearly articulate a rationale in support of the obviousness rejection, as required by the MPEP and *KSR*. The Examiner’s identification of the teachings of Stolan and Juzswik, along with the conclusory statement of “[s]uch operation would therefore have been obvious in the system of Stolan” without any rationale in support of that conclusion, does not satisfy the requirements for establishing a *prima facie* case of obviousness. Appellant notes herein that the Examiner also does not provide any explicit statement of the Examiner’s rationale for the obviousness rejection in the Advisory Action of April 21, 2010.

Assuming (because there is no explicit statement of the Examiner’s rationale in the Final Office Action and the Advisory Action) that the Examiner’s rationale is that there is some teaching, suggestion, or motivation that would have led one of ordinary skill to combine the cited references’ teachings to arrive at the claimed invention, MPEP §2143 (G) and the applicable case law require the following:

To reject a claim based on this rationale, Office personnel must resolve the *Graham* factual inquiries. Then, Office personnel must articulate the following:

- (1) a finding that there was some teaching, suggestion, or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings;
- (2) a finding that there was reasonable expectation of success; and
- (3) whatever additional findings based on the *Graham* factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

... If any of these findings cannot be made, then this rationale cannot be used to support a conclusion that the claim would have been obvious to one of ordinary skill in the art. (emphasis added).

If the Appellant’s assumption of the Examiner’s rationale as described above is correct, then the Appellant is entitled to have the foregoing required items articulated. If the Examiner’s rejection is based on some other rationale, Appellant is entitled to know what that rationale is and to be given an opportunity to respond. “The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.” MPEP §2142.

In view of the foregoing, Appellant respectfully submits that the Examiner has merely provided a conclusory statement in support of the obviousness rejection and failed to clearly articulate a rational to support his conclusion, as required by the MPEP and

KSR. Because “rejections based on obviousness cannot be sustained by mere conclusory statements,” Appellant respectfully asserts that the Examiner has failed to provide *prima facie* support for the obviousness rejection.

One skilled in the art would not combine the teachings of Stolan and Juzswik as suggested by the Examiner.

Appellant respectfully asserts that one skilled in the art would not combine the teachings of Stolan and Juzswik as suggested by the Examiner. In particular, Appellant respectfully asserts that the proposed modification of Stolan in view of Juzswik would change the principle of operation of Stolan. In addition, Appellant respectfully asserts that the proposed modification of Stolan in view of Juzswik would render Stolan unsatisfactory for its intended purpose. Furthermore, even if the proposed modification of Stolan in view of Juzswik does not change the principle of operation of Stolan and does not render the invention of Stolan unsatisfactory for its intended purpose, Appellant respectfully asserts that the proposed combination of Stolan and Juzswik would change the function of the microprocessor (12) of Stolan.

The proposed modification of Stolan in view of Juzswik would change the principle of operation of Stolan.

If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959) (see MPEP §2143.01 (VI)).

As described above, in the Final Office Action on page 3, the Examiner correctly recognizes that “Stolan does not explicitly disclose the steps of supplying a permanent energy supply from a battery unit to the monitoring module; and switching a microcontroller supply unit of the base chip to enable or disable a temporary energy supply from the battery unit to the microcontroller unit.” The Examiner then alleges that “Juzswik discloses using this technique [col. 2, line 32 – col. 3, line 4] for the purpose of reducing power consumption in a system having a microprocessor and a watchdog timer”

and concludes that “[s]uch operation would therefore have been obvious in the system of Stolan.”

Stolan discloses a system that includes the microprocessor (12) and a watchdog timer circuit (10). (See Figs. 1 and 2, and column 4, lines 43-65 of Stolan). Stolan further discloses that the watchdog timer circuit (10) includes a counter (18) and that the microprocessor (12) is programmed to check a most significant bit (MSB) status of the counter (18) every millisecond. (See column 4, line 58 of Stolan). Additionally, Stolan discloses that if the MSB is found not to be logic high, the microprocessor (12) sends a count up signal to the counter (18) and exits the counter checking program and that if the MSB is found to be logic high, the microprocessor (12) sends a count down signal to the counter (18) and exits the counter checking program to prevent an undesired reset of the microprocessor (12). (See Fig. 3 and column 5, lines 31-45 of Stolan). That is, the principle of operation of Stolan involves the microprocessor (12) checking the watchdog timer circuit (10) every millisecond to prevent an undesired reset of the microprocessor (12).

Juzswik teaches a system for controlling body electrical requirements of an automotive vehicle and monitoring various essential switch conditions to ascertain the level of activity. (See column 2, lines 31-35 of Juzswik). Juzswik further teaches that after the system enters the "sleep" mode, the system will wake up briefly some 600 or 700 milliseconds later and repower the control system sufficiently to again check the essential inputs and return to another sleep mode if no activity has occurred to conserve power. (See column 1, lines 9-11 and column 3, lines 13-18 of Juzswik). That is, Juzswik teaches that the system for monitoring the essential switch conditions sleeps and then wakes up after 600 or 700 milliseconds to conserve power.

Thus, if the system of Stolan is modified using the technique of entering and exiting the "sleep" mode, as taught by Juzswik, the proposed modification of Stolan in view of Juzswik would result in that the microprocessor (12) checks the MSB status of the counter (18) in the watchdog timer circuit (10) after 600 or 700 milliseconds of sleep.

Therefore, the proposed modification of Stolan in view of Juzswik would change the principle of operation of Stolan, which involves the microprocessor (12) checking the watchdog timer circuit (10) every millisecond to prevent an undesired reset of the

microprocessor (12). Because the proposed modification of Stolan in view of Juzswik would change the principle of operation of Stolan, Appellant respectfully asserts that the teachings of Stolan in view of Juzswik are not sufficient to render claim 1 *prima facie* obvious.

On pages 5 and 6 of the Final Office Action, the Examiner asserts that the proposed modification of Stolan in view of Juzswik does not change the principle of operation of Stolan. In particular, on page 6 of the Final Office Action, the Examiner states that “[a]pplicant’s argument appears to be that any modification made to a primary reference that changes its operation constitutes a change to its principle of operation. If that were the case, no two references could ever be properly combined.” However, Appellant has never stated that “any modification made to a primary reference that changes its operation constitutes a change to its principle of operation,” as accused by the Examiner. As described above, the proposed modification of Stolan in view of Juzswik would change the principle of operation of Stolan, which involves the microprocessor (12) checking the watchdog timer circuit (10) every millisecond to prevent an undesired reset of the microprocessor (12). MPEP §2143.01 (VI) clearly states that if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. In the case hand, the proposed modification of Stolan in view of Juzswik does change the principle of operation of Stolan, as explained above. Thus, the teachings of Stolan and Juzswik are not sufficient to render claim 1 *prima facie* obvious.

The proposed modification of Stolan in view of Juzswik would render Stolan unsatisfactory for its intended purpose.

If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984) (see MPEP §2143.01(V)).

As described above, Stolan discloses a system that includes the microprocessor (12) and the watchdog timer circuit (10), which includes the counter (18). Stolan further

discloses that the microprocessor (12) is programmed to check a most significant bit (MSB) status of the counter (18) every millisecond to prevent an undesired reset of the microprocessor (12). (See Fig. 3 and column 5, lines 31-45 of Stolan). That is, the intended purpose of Stolan is to prevent an undesired reset of the microprocessor (12) by checking the watchdog timer circuit (10) every millisecond by the microprocessor (12). As described above, Juzswik teaches that a system for monitoring essential switch conditions sleeps and then wakes up after 600 or 700 milliseconds.

Thus, if the system of Stolan is modified using the technique of entering and exiting the “sleep” mode, as taught by Juzswik, the proposed modification of Stolan in view of Juzswik would result in that the microprocessor (12) checks the MSB status of the counter (18) in the watchdog timer circuit (10) after 600 or 700 milliseconds of sleep. As a result, the modification of Stolan in view of Juzswik will make it impossible that the watchdog timer circuit (10) is checked every millisecond by the microprocessor (12) to prevent an undesired reset of the microprocessor (12). Therefore, the microprocessor (12) cannot timely send a count down signal to the counter (18) of the watchdog timer circuit (10) to prevent an undesired reset of the microprocessor (12). As a result, the counter (18) will undesirably reset the microprocessor (12) and render both the watchdog timer circuit (10) and the microprocessor (12) ineffective.

Therefore, Appellant respectfully submits that the proposed modification of Stolan in view of Juzswik would render Stolan unsatisfactory for its intended purpose of continuously monitoring the operation of the microprocessor (12) to prevent an undesired reset of the microprocessor (12). Because the proposed modification of Stolan in view of Juzswik would render Stolan unsatisfactory for its intended purpose, Appellant respectfully asserts that there is no suggestion or motivation to make the proposed modification of Stolan in view of Juzswik.

Accordingly, the proposed modification of Stolan in view of Juzswik would change the principle of operation of Stolan and would also render the invention of Stolan unsatisfactory for its intended purpose. Thus, Appellant respectfully asserts that one skilled in the art would not find sufficient teaching or suggestion to modify Stolan in view of Juzswik. Because one skilled in the art would not find sufficient teaching or

suggestion to modify Stolan in view of Juzswik, Appellant respectfully asserts that claim 1 is not obvious over Stolan in view of Juzswik.

The proposed combination of Stolan and Juzswik would change the function of the microprocessor (12) of Stolan.

Even if the proposed modification of Stolan in view of Juzswik does not change the principle of operation of Stolan and does not render the invention of Stolan unsatisfactory for its intended purpose, Appellant respectfully asserts that the proposed combination of Stolan and Juzswik would change the function of the microprocessor (12) of Stolan, and thus is not obvious to do so.

As noted in MPEP §2143.02:

“A rationale to support a conclusion that a claim would have been obvious is that all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded nothing more than predictable results to one of ordinary skill in the art. *KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, ___, 82 USPQ2d 1385, 1395 (2007); *Sakraida v. AG Pro, Inc.*, 425 U.S. 273, 282, 189 USPQ 449, 453 (1976); *Anderson's-Black Rock, Inc. v. Pavement Salvage Co.*, 396 U.S. 57, 62-63, 163 USPQ 673, 675 (1969); *Great Atlantic & P. Tea Co. v. Supermarket Equipment Corp.*, 340 U.S. 147, 152, 87 USPQ 303, 306 (1950).” (emphasis added)

As described above, Stolan discloses a system that includes the microprocessor (12) and the watchdog timer circuit (10), which includes the counter (18). Stolan further discloses that the microprocessor (12) is programmed to check a most significant bit (MSB) status of the counter (18) every millisecond to prevent an undesired reset of the microprocessor (12). (See Fig. 3 and column 5, lines 31-45 of Stolan). That is, Stolan teaches that the function of the microprocessor (12) involves checking the watchdog timer circuit (10) every millisecond. In addition, Juzswik teaches that the function of the system for monitoring the essential switch conditions involves sleeping and then waking up after 600 or 700 milliseconds to conserve power.

Thus, if the microprocessor (12) of Stolan is combined with the system for monitoring the essential switch conditions of Juzswik, the function of the microprocessor (12) of Stolan would be changed from checking the MSB status of the counter (18) in the

watchdog timer circuit (10) every millisecond to checking the MSB status of the counter (18) in the watchdog timer circuit (10) after 600 or 700 milliseconds of sleep.

Therefore, Appellant respectfully submits that the proposed combination of Stolan and Juzswik would change the function of the microprocessor (12) of Stolan. Because the proposed combination of Stolan and Juzswik would not result in elements with no change in their respective functions, Appellant respectfully asserts that one skilled in the art would not have reasonable expectation of success of combining Stolan and Juzswik. Because one skilled in the art would not have reasonable expectation of success of combining Stolan and Juzswik, Appellant respectfully asserts that claim 1 is not obvious over Stolan in view of Juzswik.

In summary, Stolan teaches that the microprocessor (12) continuously checks the watchdog timer circuit (10) to prevent an undesired reset of the microprocessor (12) while Juzswik teaches that the system for monitoring the essential switch conditions periodically sleeps and wakes up to conserve power. Thus, the proposed combination of Stolan and Juzswik would inevitably change the principle of operation of Stolan, render the invention of Stolan unsatisfactory for its intended purpose, and change the function of the microprocessor (12) of Stolan. As a result, one skilled in the art would not combine the teachings of Stolan and Juzswik as suggested by the Examiner.

Accordingly, Appellant respectfully asserts that the Examiner has failed to provide *prima facie* support for the obviousness rejection. In addition, Appellant respectfully asserts that one skilled in the art would not combine the teachings of Stolan and Juzswik as suggested by the Examiner. Therefore, Appellant respectfully submits that a *prima facie* case of obviousness has not been established with respect to claim 1. Accordingly, Appellant respectfully asserts that claim 1 is patentable over Stolan in view of Juzswik.

B. Appellant respectfully asserts that independent claim 5 is patentable over Stolan in view of Juzswik under 35 U.S.C. 103(a).

Independent claim 5 includes similar limitations to independent claim 1. Because of the similarities between claim 5 and claim 1, Appellant respectfully asserts that the remarks provided above with regard to claim 1 apply also to claim 5. Thus, Appellant

respectfully asserts that the Examiner has failed to provide *prima facie* support for the obviousness rejection. In addition, Appellant respectfully asserts that one skilled in the art would not combine the teachings of Stolan and Juzswik as suggested by the Examiner. Therefore, Appellant respectfully submits that a *prima facie* case of obviousness has not been established with respect to claim 5. Accordingly, Appellant respectfully asserts that claim 5 is patentable over Stolan in view of Juzswik.

C. Appellant respectfully asserts that dependent claims 3, 4 and 6-13 are patentable over Stolan in view of Juzswik under 35 U.S.C. 103(a) or patentable over Stolan in view of Juzswik and further in view of Ubicom under 35 U.S.C. 103(a)

Given that claims 3, 4 and 6-13 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 5, Appellant respectfully submits that claims 3, 4 and 6-13 are allowable at least based on allowable claims 1 and 5.

Additionally, each of claims 3, 4 and 6-13 may be allowable for further reasons.

VIII. CONCLUSION

A *prima facie* case of obviousness has not been established with respect to independent claims 1 and 5. Thus, independent claim 1 and 5 are not obvious over Stolan in view of Juzswik. In addition, dependent claims 3, 4 and 6-13 are allowable at least based on allowable claims 1 and 5 since claims 3, 4 and 6-13 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 5.

For the reasons stated above, claims 1 and 3-13 are patentable over the cited references. Appellant respectfully requests that the Board reverse the rejections of claims 1 and 3-13.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

Date: September 9, 2010

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IX. CLAIMS APPENDIX

Listing of Claims:

1. A method of monitoring the operation of a microcontroller unit that is intended for at least one application and is associated with a system, by means of a base chip, particularly a system base chip, characterized in that:

causing a reset of the microcontroller unit if a reset condition is detected, wherein the reset condition is transmission of at least one special sequence, particularly at least one drive or access sequence assigned to the reset operation, to the base chip and the reset of the microcontroller unit is confirmed under an enquiry routine by checking whether the at least one special sequence has been successfully transmitted to the base chip;

activating a special mode of operation, particularly a flash mode of the base chip, once after the check has been made to see whether the special sequence has been successfully applied and after the reset operation, by allowing access to a monitoring module that is associated with the base chip to take place in a manner which is simplified in comparison with the normal mode of operation of the microcontroller unit;

supplying a permanent energy supply from a battery unit to the monitoring module; and

switching a microcontroller supply unit of the base chip to enable or disable a temporary energy supply from the battery unit to the microcontroller unit.

3. A method as claimed in claim 1 further comprising:

during the special mode of operation, using a special trigger code or a special trigger signal for the monitoring module that is different from the normal mode of operation; and

causing a fresh reset of the microcontroller unit using the normal trigger code or the normal trigger signal, to enable the special mode to be exited again.

4. A method as claimed in claim 1 further comprising:

making a distinction between reset events that differ in relation to the operation of the microcontroller unit; and

logging said different reset events and making said different reset events known in at least one register unit using different register entries.

5. A base chip, particularly a system base chip, for monitoring the operation of a microcontroller unit that is intended for at least one application, characterized by:

a reset unit for resetting the microcontroller unit, which reset unit is connected to said microcontroller unit, wherein a reset of the microcontroller unit is caused if a reset condition is detected, wherein the reset condition is transmission of at least one special sequence, particularly at least one drive or access sequence assigned to the reset operation, to the base chip and the reset of the microcontroller unit is confirmed under an enquiry routine by checking whether the at least one special sequence has been successfully transmitted to the base chip;

a microcontroller supply unit connected to the microcontroller unit, wherein the microcontroller supply unit is permanently associated with a battery unit;

a switch connected to the microcontroller supply unit, wherein the switch is configured to switch the microcontroller supply unit to enable or disable a temporary energy supply from the battery unit to the microcontroller unit; and

a monitoring module that is associated with the microcontroller unit, wherein a special mode of operation, particularly a flash mode of the base chip, can be activated once after the check has been made to see whether the special sequence has been successfully applied and after the reset operation, by allowing access to the monitoring module to take place in a manner which is simplified in comparison with the normal mode of operation of the microcontroller unit, wherein the monitoring module is permanently associated with the battery unit so that the monitoring module receives a permanent energy supply from the battery unit.

6. A base chip as claimed in claim 5 further comprising:

at least one register unit configured to allow for different reset events, to log and make known different reset events using different register entries.

7. A base chip as claimed in claim 6, characterized in that:

the monitoring module is triggerable in particular by means of at least one interface unit; or

to distinguish between the particular accesses to the monitoring module, different reset events can be marked by different trigger codes or trigger signals.

8. A base chip as claimed in claim 7, characterized in that there is provided between the monitoring module and the microcontroller unit at least one signal line for transmitting at least one trigger code or trigger signal that differs from the normal mode of operation of the microcontroller unit.

9. A system, and particularly a control system, characterized by at least one microcontroller unit intended for at least one application and by at least one base chip as claimed in claim 5.

10. Use of a method as claimed in claim 1 for monitoring the operation of at least one microcontroller unit intended for at least one application, in the electronics of motor vehicles.

11. The use of a method as claimed in claim 10, wherein the at least one application includes automobile electronics.

12. Use of at least one base chip as claimed in claim 5 for monitoring the operation of at least one microcontroller unit intended for at least one application, in the electronics of motor vehicles.

13. The use of at least one base chip as claimed in claim 12, wherein the at least one application includes automobile electronics.

X. EVIDENCE APPENDIX

There is no evidence submitted with this Appeal Brief.

XI. RELATED PROCEEDINGS APPENDIX

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.